What is claimed is:

1. A method for manufacturing a MOSFET device, the method comprising:

(a) selectively forming a shallow trench isolation in a substrate;

(b) forming a first oxide layer on a surface of an active region of the substrate and implanting ions thereinto for forming a low doped drain in the active region;

(c) forming a nitride layer;

(d) removing a part of the nitride layer and the oxide layer where a gate will be located and etching the substrate corresponding to the part by a predetermined depth;

(e) forming a second oxide layer over an exposed portion of the substrate;

(f) implanting ions into the substrate;

(g) removing the second oxide layer;

(h) depositing a gate insulating layer and a polysilicon;

(i) polishing until the nitride layer is exposed;

(j) removing the nitride layer, depositing an oxide layer conformally and depositing an nitride layer;

(k) etching the nitride layer to form a gate sidewall of nitride;

(l) implanting ions into the substrate to form a source and drain at both sides of the gate; and

(m) removing an exposed oxide layer.

2. A method as defined by claim 1, wherein the substrate comprises a silicon substrate.

3. A method as defined by claim 1, wherein the shallow trench isolation comprises an oxide layer.

4. A method as defined by claim 1, wherein the predetermined depth is in range of about 200 to about 1000 angstroms.

5. A method as defined by claim 1, wherein the exposed substrate is oxidized at about 600 to about 800 °C to form the second oxide layer having a thickness of about 100 angstroms in (e).

6. A method as defined by claim 1, wherein a chemical mechanical polishing is performed in (i).

7. A method as defined by claim 1, wherein the nitride layer is removed by an etch back processing in (k).